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EXECUTIVE SUMMARY

2005-now MTS-Engineer for Google. **Design/debug server hardware** .
2003-2004 **M.S. degree** in Information and Computer Sciences from UC Irvine. GPA=3.9.
1996-2002 Principal Engineer for Systems Science, later acquired by Synopsys. **Designed/wrote/maintained CAD tools** written in C.
1988-1996 Staff Engineer (emp. #10) for MasPar Computer. **Architecture design** of the inter-processor router network. **Chip design** of 3+ full-custom CMOS chips and 1 CMOS gate array. **Board-level design** of the router network and high-speed I/O channel. **Wrote diagnostics** in C, MPL (parallel C), and microcode.
1987-1988 Contractor for Systems Science. **Wrote netlist translator** in C/lex/yacc/make.
1986-1987 Contractor for Standard Microsystems (see below).
1984-1986 Senior engineer for Silicon Solutions, now Zycad. **Designed/wrote custom CAD tools** in C. Helped with **chip design** of several full-custom CMOS chips.
1982-1983 **B.S. degree** with high honors in EE/CS from UC Berkeley. GPA=3.7.
1975-1982 Senior Engineer for Standard Microsystems. **Chip design** of 8+ full-custom NMOS chips.

EMPLOYMENT DETAILS

2005-now: Member of Technical Staff -- Engineer, **Google, Inc.**, Mountain View, CA.

Design and debug computer hardware, especially high-end server boards.

1996-2002: Engineering Project Leader, **Synopsys, Inc.**, Mountain View, CA.

Originally hired as Principal Engineer, **Systems Science, Inc.** (see below), acquired by Synopsys in 1998.

Development of CAD software for chips and systems, especially the Vera verification tool/language.

- Wrote assembly-language code to call user-defined procedures with (argc, argv) interface on Sparc-Solaris (32- and 64-bit), Linux i386, HP-UX, and DEC-Alpha systems.
- Integrated temporal-expression capabilities into Vera.
- Wrote interface between Vera and the Denali smart memory-model package.
- Implemented Java-style threads in C++ using the QuickThreads toolkit.
- Wrote interface code joining Vera to Cadence's Leapfrog and NC-VHDL logic simulators.
- Familiar with code-development tools: CVS, gmake, gdb, Purify and Pure Coverage.
- Proficient in writing and generating VHDL code; competent in Verilog.
- Wrote logic-simulation database record-playback package with editing capabilities.

1988-1996: Staff Engineer (employee #10), **MasPar Computer Corp.**, Sunnyvale, CA.

Architecture and hardware design for the MP-1, -2, and -3 massively parallel supercomputers, plus CAD and diagnostic software.

- Architecture design included inter-processor communication (router) networks and a 200-MB/s I/O channel. Presented router network and chip design at MIT's VLSI Seminar.
- Hardware design included extensive full-custom CMOS design, layout, verification, and test; a CMOS gate array; and help with several board-level logic designs.
 - Full-custom CMOS design included two generations of router chip, a bus-interface transceiver (BIX chip), and the SRAM and multiplier sections of several processor-element chips. Several of these designs included some way-cool analog circuitry!
 - Did the layout of the BIX chip using Cadence Edge tools.
 - The gate array (ChIL chip) implemented the I/O-channel protocol.
 - Board design included the instruction-fetch section of the MP-1 control board, and the channel-interface sections of several I/O boards.
 - Hardware experience also included leadership in the bring-up and debug of the MP-1, plus other guru-level h/w debugging, including transmission-line effects and some very subtle I/O-system e-mag problems.
- Design-aid software included router architecture simulators, some Synopsys VHDL and CLI modelling, UNIX glue for inhomogeneous tools, and extensive Cadence Skill and DRC scripts for CMOS synthesis and verification. Used Cadence Edge, Epic PathMill, and several Zycad logic- and fault-simulation accelerators.
- Diagnostic software included comprehensive router and I/O-channel tests and MasPar's universal memory-test program met. Learned data-parallel programming and wrote a 200k-crypts/s UNIX password cracker.

1987-1988: Contractor, **Systems Science, Inc.**, Menlo Park, CA.

Wrote NECSIM netlist translator: NEC proprietary formats into EDIF. Compiler-like project included LEX and YACC, plus hash- and symbol-table, semantic analysis, and code-generator modules.

1986-1987: Contractor, **Standard Microsystems Corp.** (see below).

Helped with several projects while trying to establish a full-time California-based employment arrangement. Tasks included yield improvement and process troubleshooting, plus back-end work on 84C19/28/29 DRAM controller and 84C02/03/04/05 ECC chip. Did layout editing on a Calma GDS-II. Wrote a switch-level logic simulator for the IBM PC.

1984-1986: Senior Engineer, **Silicon Solutions Corp.**, Menlo Park, CA (now **Zycad**).

System/board/chip design work on the MACH-1000 logic/fault-simulation hardware accelerator. Learned simulation algorithms. Wrote the architecture simulator for the accelerator. Helped with design and layout of custom CMOS chips.

1975-1982: Senior MOS Design Engineer, **Standard Microsystems Corp.**, Hauppauge, NY.

Started as Technician and was quickly promoted to Engineer. Designed the following chips:

- 9216 and 9229 floppy-disk data separators
- 9003 floppy-disk controller
- 1863, 8017, and 8018 UARTs
- 8004 SDLC-specific CRC generator/checker
- 8046, 8116/26/36/46, and 8216 baud-rate generators
- Also worked on 1671 (Astro) and 5025/35 (SDLC) USARTs.

- Other contributions included design of single-pin crystal oscillators for N- and C-MOS processes and software for finite-state machine emulation and circuit simulation.

EDUCATION

2003-2004: Ph.D. student on leave of absence from **University of California, Irvine** School of Information and Computer Sciences. Area of concentration: Computer Systems and Networks, especially Networks on Chip. Master of Science degree conferred 2005 March 24. GPA = 3.9 / 4.0.

1982-1983: **University of California, Berkeley** : Bachelor of Science with High Honors in EE/CS. Did graduate-level work on CMOS version of SOAR (Smalltalk On A RISC) microprocessor. GPA = 3.7 / 4.0.

1968-1970: **Rensselaer Polytechnic Institute** , Troy, NY: two years of pre-engineering.

1964-1968: Riverhead (NY) High School: Graduated 2nd in class of 215. SAT scores: 701 verbal, 759 math.

PATENTS

- 5,598,408 (1997); 5,280,474 (1994) and 5,243,699 (1993) Router network architecture
- 5,488,694 (1996) I/O-channel architecture
- 5,450,330; 5,434,977 (1995) and 5,345,556 (1994) Router chip circuitry
- 4,516,040 (1985) and 4,409,499 (1983) High-speed merged-plane PLA
- 4,472,818 (1984) Floppy-disk data separator
- 4,433,253 (1984) Three-phase regulated high-voltage charge pump

OTHER QUALIFICATIONS

High-level languages : expert in C; very experienced in Perl, sh/csh, make, and other UNIX tools; competent in Java and Pascal; limited experience in C++, Snobol and APL; experienced but rusty in (old) Fortran, PL/I, and Basic. Allergic to COBOL!

Have written programs in many **assembly languages** including DEC Alpha, VAX, PDP-11, PDP-10, and PDP-8; Sun SPARC; HP MIPS and 21-MX; Motorola 6800 and 68000; Intel 8080 and 8086/88; Zilog Z-80; MasPar MP-1/2; DG NOVA; IBM 360; Prime 300; and Nuclear Data ND-812.

Owner and system administrator of **jzap.com** running on a Sparc-Solaris machine. Wrote CGI scripts to serve and interactively update NHL hockey standings. Wrote software to receive ham-radio competition logs via e-mail, including CGI script to serve entrants their password-protected logs. Compiled/installed V8 Sendmail and hacked the C-code to prevent open relay of spam; also successfully completed some non-trivial hacks to sendmail.cf! Compiled/installed many other free-software packages including the apache web server; the named DNS server; IP utilities sock, tcpdump and traceroute; etc.

Ham-radio operator (K2MM / WA1MUG) since 1967 (Extra Class 1970). Have designed, built, and operated repeaters (144 and 440 MHz); plus assorted receivers, transmitters, amplifiers, antennas, etc. Have written IBM-PC code for ham-radio TCP/IP, including a context scheduler for multi-threading within a single Turbo-C program. Enjoy radiosport contesting, especially VHF/UHF mountain-topping and high-speed Morse code. FCC First-Class Radiotelephone license since 1969.